4. (amended) A semiconductor device having a non-volatile memory transistor according to claim 2, wherein the semiconductor substrate is a p-type, the first well is an n-type, the second well is a p-type, and each of the source and drain is an n-type.

6. (amended) A semiconductor device having a non-volatile memory transistor having a split-gate structure, the semiconductor device comprising:

a semiconductor substrate of a first conductivity type having a memory region;

a first well of a second conductivity type located in the memory region; and

a second well of a first conductivity type located in the first well, wherein the non-volatile memory transistor includes a source and drain that are located in the second well;

wherein the non-volatile memory transistor is operated using voltages including positive and negative voltages;

wherein, for writing data in the non-volatile memory transistor, a voltage in an opposite polarity is applied to the control gate, a voltage in one polarity is applied to one of the source and the drain, a voltage in the opposite polarity is applied to the other of the source and the drain, a voltage in the opposite polarity is applied to the second well, and a voltage in the one polarity is applied to the first well;

wherein, for erasing data in the non-volatile memory transistor, a voltage in the one polarity is applied to the control gate, a voltage in the opposite polarity is applied to one of the source and the drain, a voltage in the opposite polarity is applied to the other of the source and the drain, a voltage in the opposite polarity is applied to the second well, and a voltage in the one polarity is applied to the first well;

wherein, for writing data in the non-volatile memory transistor, a voltage of –3 V through –4 V is applied to the control gate, a voltage of +3 V through +4 V is applied to one of the source and the drain, a voltage of –5 V through –6 V is applied to the other of the source and the drain, a voltage of –5 V through –6 V is applied to the second well, and a voltage of +0.9 V through +3.3 V is applied to the first well; and

wherein, for erasing data in the non-volatile memory transistor, a voltage of +6 V through +7 V is applied to the control gate, a voltage of –5 V through –6 V is applied to one of the source

and the drain, a voltage of –5 V through –6 V is applied to the other of the source and the drain, a voltage of –5 V through –6 V is applied to the second well, and a voltage of +0.9 V through +3.3 V is applied to the first well.

9. (amended) A semiconductor device having a non-volatile memory transistor according to claim 1, wherein the non-volatile memory transistor has a gate insulation layer, a floating gate, a control gate and an intermediate insulation layer functioning as a tunnel insulation layer, wherein

the gate insulation layer is located above the second well and between one of the source and drain and the other of the source and drain,

the floating gate is located above the first gate insulation layer,

the intermediate insulation layer is located above the floating gate and the semiconductor substrate, and

the control gate is located above the intermediate insulation layer and rests on the floating gate through the intermediate insulation layer.

15. (amended) A semiconductor device having a non-volatile memory transistor according to claim 14, wherein the insulation layer between the first and second outermost layers that is formed by a CVD method is a silicon oxide layer formed by a CVD method selected from a group consisting of a HTO (high temperature oxide) method and a TEOS (tetraethyl orthosilicate) method.

22. (amended) A semiconductor device having a non-volatile memory transistor according to claim 14, wherein the first outermost layer that forms the intermediate insulation layer of the non-volatile memory transistor has a film thickness of 5 – 15 nm, and the second outermost layer has a film thickness of 1 – 10 nm, and the layer formed between the first and the second outermost layers comprises a silicon oxide layer having a film thickness of 10 – 20 nm.

24. (amended) A semiconductor device having a non-volatile memory transistor having a split-gate structure, the semiconductor device comprising:

a semiconductor substrate of a first conductivity type having a memory region;

a first well of a second conductivity type located in the memory region;

a second well of a first conductivity type located in the first well, wherein the non-volatile memory transistor includes a source and drain that are located in the second well;

wherein the non-volatile memory transistor has a first gate insulation layer, a second gate insulation layer, a floating gate, a control gate and an intermediate insulation layer functioning as a tunnel insulation layer;

wherein the first gate insulation layer and the second gate insulation layer are located above the second well and between one of the pair of source and drain and the other of the pair of source and drain, the floating gate is located above the first gate insulation layer, the intermediate insulation layer is located above the floating gate, and the control gate is located above the second gate insulation layer and rests on the floating gate through the intermediate insulation layer;

wherein the semiconductor substrate includes first, second and third transistor regions including field effect transistors that operate at different voltage levels, wherein the first transistor region includes a first voltage-type transistor that operates at a first voltage level of 1.8 - 3.3 V, the second transistor region includes a second voltage-type transistor that operates at a second voltage level of 2.5 - 5 V, and the third transistor region includes a third voltage-type transistor that operates at a third voltage level of 10 - 15 V; and

wherein the second voltage-type transistor has a gate insulation layer formed from at least two insulation layers, and includes an insulation layer that is formed in the same step in which a gate insulation layer of the first voltage-type transistor is formed.

25. (amended) A semiconductor device having a non-volatile memory transistor according to claim 10, further comprising at least a flash-memory (flash EEPROM), wherein the flash-memory includes a memory cell array comprising non-volatile memory transistors and peripheral circuits formed therein.

26. (amended) A semiconductor device having a non-volatile memory transistor according to claim 25, further comprising another circuit region mixed together with the flash-memory (flash EEPROM) on the substrate.

27. (amended) A semiconductor device having a non-volatile memory transistor according to claim 26, wherein the circuit region includes at least a logic circuit.

Please add new claims 33-34 as follows:

33. A semiconductor device according to claim 1, wherein

wherein the semiconductor substrate further includes first, second and third transistor regions including first, second and third field effect transistors that operate at different voltage levels, the second field effect transistor including a gate insulation layer formed from two silicon oxide layers, and the third field effect transistor including a gate insulation layer formed from three silicon oxide layers.

34. A semiconductor device according to claim 31, wherein the second layer of the intermediate insulation layer is silicon oxide.

REMARKS

Applicant has amended claims 1, 4, 6, 9, 15, 22 and 24-27 and added new claims 33-34. Claims 1-34 are currently pending. Reexamination and reconsideration are respectfully requested.

The title was objected to by the Examiner. Applicant has proposed a new title as set forth above.

Claims 15, 22, 26 and 27 were rejected under 35 U.S.C. 112 as being indefinite. Claims 15 and 22 have been amended to ensure that adequate antecedent basis has been provided. Claim 26 (from which claim 27 depends) has been amended for clarity. Applicant respectfully submits that claims 15, 22, 26 and 27 comply with section 112.

Claims 1-5, 7, 9, 23 and 32 were rejected under 35 U.S.C. 102(b) as unpatentable over